In the Claims

1.   (Currently Amended) A semiconductor processing method, comprising:

forming an insulative mass across a first electrical node and a second electrical node; the mass having a pair of openings extending therethrough to the electrical nodes, the insulative mass having an outermost surface proximate the openings; the individual openings each having a periphery defined by at least a portion of one of the electrical nodes and at least one sidewall; one of the openings extending to the first electrical node and being a first opening, and the other of the openings extending to the second electrical node and being a second opening;

forming at least one isolation region laterally adjacent at least one of the first and second electrical nodes, the isolation region having a thickness that is less than a thickness of the at least one of the first and second electrical nodes;

forming a dielectric material layer within the openings to narrow the openings, the dielectric material layer lining the at least one sidewall of the first and second openings; and

forming conductive material plugs within the narrowed openings; the conductive material plug within the first opening being a first conductive material plug and being separated from the first electrical node by the dielectric material, and the conductive material plug within the second opening being a second conductive material plug and not being separated from the second electrical node by the dielectric material, wherein after forming the conductive material plugs, the dielectric material layer lining the at least one sidewall of the second opening is formed to be coplanar with the outermost surface

proximate the second opening, and the outermost surface of the insulative mass proximate the first and second openings being coplanar.

2.   (Original) The method of claim 1 wherein the insulative mass comprises borophosphosilicate glass.

3.   (Original) The method of claim 1 wherein the dielectric material layer comprises silicon nitride.

4.   (Original) The method of claim 1 wherein the dielectric material layer comprises silicon oxynitride.

5.   (Original) The method of claim 1 wherein the dielectric material layer comprises silicon nitride and is formed to a thickness of from about 30Å to about 100Å.

6.   (Original) The method of claim 1 wherein the first electrical node comprises a p-type doped diffusion region within a semiconductive material.

7.   (Original) The method of claim 1 wherein the first electrical node comprises an n-type doped diffusion region within a semiconductive material.

8. (Original) The method of claim 1 wherein the first electrical node comprises a metal.

9. (Original) The method of claim 1 wherein the first electrical node comprises copper.

10. (Original) The method of claim 1 wherein the first electrical node comprises aluminum.

11. (Original) The method of claim 1 wherein the first electrical node comprises copper and aluminum.

12. (Original) The method of claim 1 wherein the conductive plugs comprise conductively doped silicon.

13. (Original) The method of claim 1 wherein the conductive plugs comprise a metal.

14. (Original) The method of claim 1 wherein the conductive plugs comprise tungsten.

15.   (Original) The method of claim 1 wherein the conductive plugs comprise copper.

16.   (Original) The method of claim 1 wherein the conductive plugs comprise aluminum.

17.   (Original) The method of claim 1 wherein the conductive plugs comprise copper and aluminum.

18.   (Original) The method of claim 1 wherein the conductive plugs comprise a layer of titanium nitride against the dielectric material; and a mass of tungsten over the layer of titanium nitride.

19.   (Original) The method of claim 1 wherein the conductive plugs comprise a composite layer of titanium and titanium nitride against the dielectric material; and a mass of tungsten over the composite layer of titanium and titanium nitride.

20.   (Currently Amended) A semiconductor processing method, comprising:

forming an insulative mass across a first electrical node and a second electrical node; the first electrical node being within a substrate region, the first electrical node comprising a first-type dopant, and the second electrical node being within a substrate region, the second electrical node comprising a second-type dopant different from the first-type dopant; the mass having a pair of openings extending therethrough to the electrical nodes, the insulative mass having an outermost surface proximate the openings; the individual openings each having a periphery defined by at least a portion of one of the electrical nodes and at least one sidewall; one of the openings extending to the first electrical node and being a first opening, and the other of the openings extending to the second electrical node and being a second opening;

forming a dielectric material layer within the openings to narrow the openings; and

forming conductive material plugs within the narrowed openings; the conductive material plug within the first opening being a first conductive material plug and not being in electrical contact with the first electrical node, and the conductive material plug within the second opening being a second conductive material plug and being in electrical contact with the second electrical node, wherein after forming the conductive material plugs, the first and second openings have substantially equal widths from the periphery defined by at least a portion of one of the electrical nodes to the outermost surface of the insulative mass, the outermost surface proximate the first and second openings being coplanar.

21.   (Original) The method of claim 20 wherein the insulative mass comprises borophosphosilicate glass.

22.   (Original) The method of claim 20 wherein the dielectric material layer comprises silicon nitride.

23.   (Original) The method of claim 20 wherein the dielectric material layer comprises silicon nitride and is formed to a thickness of from about 30Å to about 100Å.

24.   (Currently Amended) A semiconductor processing method, comprising:

providing a semiconductor substrate having a pair of electrical nodes supported

thereby; the electrical nodes being a first electrical node and a second electrical node,

respectively;   ʄ

forming an insulative mass over the substrate; the mass having a pair of openings

extending therethrough to the electrical nodes, the insulative mass having an outermost

surface proximate the openings; the individual openings each having a periphery defined

by a bottom and at least one sidewall; the opening extending to the first electrical node

being a first opening, and the opening extending to the second electrical node being a

second opening;

~~forming at least one isolation region laterally adjacent at least one of the first and~~

~~second electrical nodes, the isolation region having a thickness that is less than a~~

~~thickness of the at least one of the first and second electrical nodes;~~

forming a dielectric material layer within the openings to narrow the openings; the

dielectric material layer lining the at least one sidewall and bottom of the first opening, and

lining the at least one sidewall but not a predominant portion of the bottom of the second

opening;

forming conductive material plugs within the narrowed openings; the conductive

material plug within the first opening being a first conductive material plug, and the

conductive material plug within the second opening being a second conductive material

plug, wherein after forming the conductive material plugs, the dielectric material layer lining

the at least one sidewall of the second opening being formed to be coplanar with the

outermost surface of the insulative mass proximate the second opening, and the outermost

surface proximate the first and second openings being coplanar; and

wherein the conductive plugs comprise a layer of titanium nitride against the

dielectric material; and a mass of tungsten over the layer of titanium nitride.

25.   (Original) The method of claim 24 wherein an anti-fuse is defined by the first

electrical node together with the dielectric material layer in the first opening and the first

conductive material plug; and further comprising providing sufficient power to the anti-fuse

to electrically connect the first electrical node and first conductive material plug to one

another.

26.   (Original) The method of claim 24 wherein the forming the dielectric material

layer comprises:

forming the dielectric material layer along the at least one sidewall of the second

opening and along the bottom of the second opening while forming the dielectric material

layer along the at least one sidewall and along the bottom of the first opening;

forming a protective mask over the first opening and leaving the second opening

uncovered by the protective mask; and

while the protective mask is over the first opening; anisotropically etching the

dielectric material layer from over the predominant portion of the bottom of the second

opening.

27.   (Original)   The method of claim 24 wherein the dielectric material layer comprises silicon nitride.

28.   (Original)   The method of claim 24 wherein the dielectric material layer comprises silicon nitride and is formed to a thickness of from about 30Å to about 100Å.

29.   (Original) The method of claim 24 wherein the first electrical node comprises a p-type doped diffusion region within a semiconductive material of the semiconductor substrate.

30.   (Original) The method of claim 24 wherein the first electrical node comprises an n-type doped diffusion region within a semiconductive material of the semiconductor substrate.

31.   (Original) The method of claim 24 wherein the first electrical node comprises a metal.

32.   (Original) The method of claim 24 wherein the first electrical node comprises copper.

33.   (Original) The method of claim 24 wherein the first electrical node comprises aluminum.

34. (Original) The method of claim 24 wherein the first electrical node comprises copper and aluminum.

35. (Original) The method of claim 24 wherein the conductive plugs comprise conductively doped silicon.

36. (Original) The method of claim 24 wherein the conductive plugs comprise a metal.

37. (Original) The method of claim 24 wherein the conductive plugs comprise tungsten.

38. (Original) The method of claim 24 wherein the conductive plugs comprise copper.

39. (Original) The method of claim 24 wherein the conductive plugs comprise aluminum.

40. (Original) The method of claim 24 wherein the conductive plugs comprise copper and aluminum.

Claims 41-59 (Cancelled).